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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,778	12/10/2001	Ravindra Karnad	TI-31646	3367

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,778	KARNAD, RAVINDRA	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *8-12,17-22 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,13-16 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-7, 13-16, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boudreaux, Jr. (US Patent 6,668,060) in view of Anderson et al. (US Patent 6,728,370).**

Claim 1 is limited to *a subscriber loop interface circuit.* Boudreaux discloses a tracking switch-mode power converter for a telephony interface circuit (i.e. *subscriber loop interface circuit*). See Abstract. Figures 1 and 2 depict the general circuitry used in supplying a DC current feed to a telephone line (20), whose ultimate destination is represented as load R_p. A detailed implementation of the current feed circuitry depicted in figure 2 is shown in figure 3. It will become apparent that the configuration depicted in figure 3 contains the same elements and orientation as those components depicted in figure 17 of the instant application, and as such, the circuit of Boudreaux will achieve *at least 80% efficiency.* It is clear from figure 3, that the output of the converter is a DC signal, conditioned to be so by inductor (160). The presence of this inductor inherently establishes a high-impedance to voice band signals. In addition to disclosing the presence of DC current on the tip and ring lines (20), Boudreaux also discloses that AC signals are superimposed with said DC current; see column 1, lines 49-62. This disclosure provides evidence for some type of *AC current source*, however, it is clear

that Boudreaux does not provide an enabling disclosure to one of ordinary skill in the art as to how to implement this *AC*/voice *current source*.

In order to remedy the above deficiency, one of ordinary skill in the art would be inherently motivated to find an enabling disclosure for said *AC current source*. Anderson teaches a method and apparatus for impedance matching. See Abstract. Figure 4 depicts hybrid circuitry for a telephone interface circuit, like that of Boudreaux. The hybrid circuitry includes a driver (105) that drives a downstream voice component (465) through resistor (404). Resistor (404) provides the dual purpose of providing subscriber loop impedance matching and current sensing. Furthermore, signal adder (402) filters the downstream voice (465) using an impedance matched voice signal so as to better match the subscriber loop impedance as it varies. See figure 2 for general operation. It would have been obvious to one of ordinary skill in the art to combine the teachings of Anderson directed toward an impedance matching *AC current source* with the DC current source of Boudreaux for the purpose of enabling the implementation of an *AC current source* for superimposed voice.

Claim 2 is limited to *the subscriber loop interface circuit according to claim 1*, as covered by Boudreaux in view of Anderson. The tracking switch-mode power supply depicted in figure 3 of Boudreaux clearly corresponds to the circuitry depicted in figure 17 of the instant application. In particular, the presence of the charging capacitor (162) provides boost current to the output inductor (160) during periods when switch-mode transistor (150) is conductive. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 3 is limited to *the subscriber loop interface circuit according to claim 2*, as covered by Boudreaux in view of Anderson. As seen in figure 3, Boudreaux includes *a first semiconductor switch* (150) and *a second semiconductor switch* (164). Analysis of the circuitry indicates that when the *first switch* (150) is conductive, a negative potential is present at the anode of the *second switch* (164), causing reverse bias and placing the second switch into a cut-off (i.e. *open*) mode. This corresponds to the *second state*. When the *first switch* (150) is not conducting current, the ground is used to sink current that is sourced by the output inductor (160). This corresponds to the *first state*. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 4 is limited to *the subscriber loop interface circuit according to claim 3*, as covered by Boudreaux in view of Anderson. Figure 3 depicts a capacitor (162) whose position clearly indicates that it charges during the first state because of the bias supplied by the –48V battery. Thus, it must discharge during the second state as transistor (150) conducts. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 5 is limited to *the subscriber loop interface circuit according to claim 4*, as covered by Boudreaux in view of Anderson. Figure 3 also depicts an output inductor comprising elements (160) and (132). Clearly, as the output is DC, voice signals that may leak onto the output line will meet a high-impedance. With respect to limiting output current ripple to less than about one percent, there is no disclosure within Boudreaux pertaining to the amount of high-frequency switch-mode ripple the output inductors remove.

It has been found that changes in size/proportion that do not effect the overall operation of the art to be obvious; see In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); and Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984). Because the impedance of an inductor can be related by the equation $z = j\omega L$, it is clear that the result of increasing the size of an output inductor is reduction in ripple. The instant claim suggests scaling the output inductor to reduce ripple to less than about one percent, while the prior art only indicates selecting a suitable scaling to generate DC. It follows that the only difference that can be construed between the instant claim and the prior art is one relating to a change in size/proportion, whose result merely reduces ripple at the output of the circuit, while the function of the circuit is essentially the same. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 6 is limited to *the subscriber loop interface circuit according to claim 5*, as covered by Boudreaux in view of Anderson. As seen in figure 3, the *first switch* (150) is really a *CMOS transistor*. It receives an input from operational amplifier (100) that acts as a comparator to selectively activate the transistor (150) according to the dynamic and time-varying voltage state of the tip and ring lines (20); see column 4, line 58 through column 5, line 2. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 7 is limited to *the subscriber loop interface circuit according to claim 6*, as covered by Boudreaux in view of Anderson. As seen in figure 3, the *second switch*

(164) is really a *fast-response diode*. As explained in the rejection of claim 2, it operates in an alternate fashion to *the first switch*, which was shown in the rejection of claim 6 to be controlled by a *dynamically time varied input signal*. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 13 is limited to *a subscriber loop interface circuit* that comprises elements already described in claim 5, as covered by Boudreaux in view of Anderson. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claims 14-16 are essentially the same as claims 5-7, respectively, and are rejected for the same reasons.

Claim 23 is limited to *a method of generating a subscriber line constant DC current feed*. The subscriber loop interface circuit recited in claim 5 inherently performs the method steps of the instant claim. Therefore, Boudreaux in view of Anderson makes obvious all limitations of the claim.

Claim 25 is limited to *a subscriber loop interface circuit* that is essentially the same as claim 1, and is rejected for the same reasons.

Response to Arguments

Applicant's arguments filed 25 April 2005 have been fully considered but they are not persuasive.

Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically

pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
9/8/05

SINH TRAN
SUPERVISORY PATENT EXAMINER